

AI驅動之光子與電子IC設計

AI-Driven Photonic-Electronic Integrated Circuit Design

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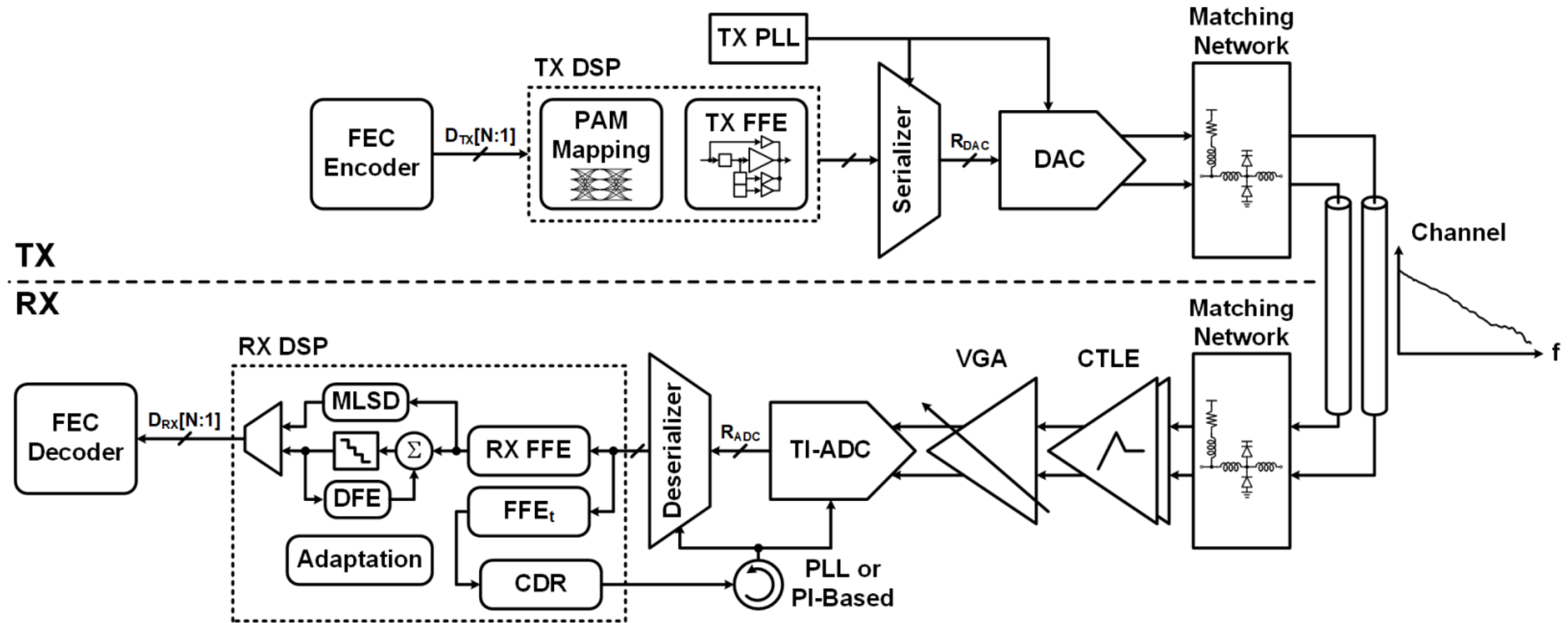
黃正良

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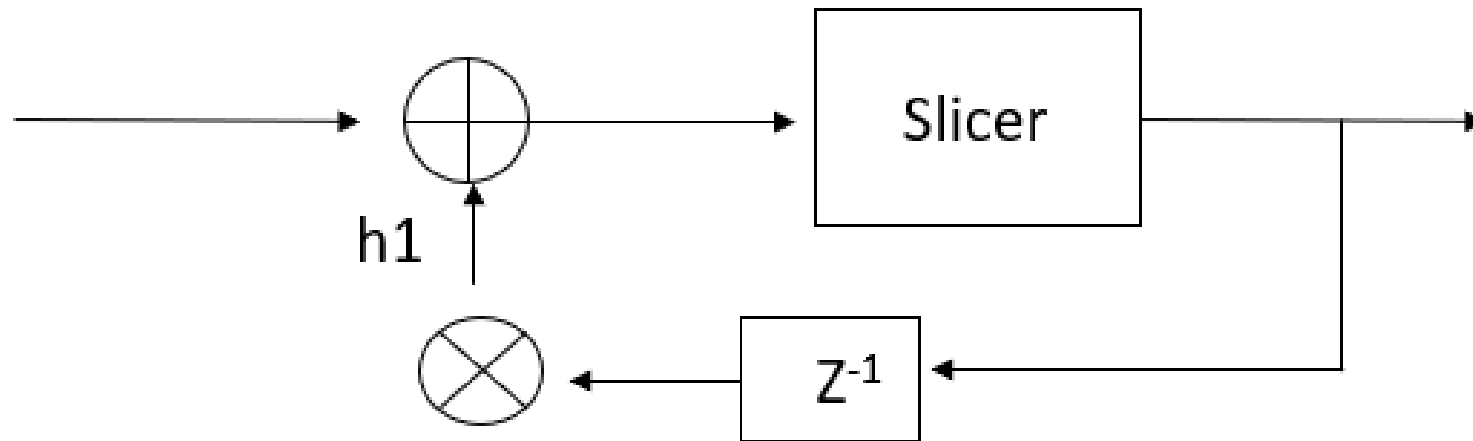
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DAC/ADC-DSP-based wireline transceiver



DFE— The Real Timing Bottleneck

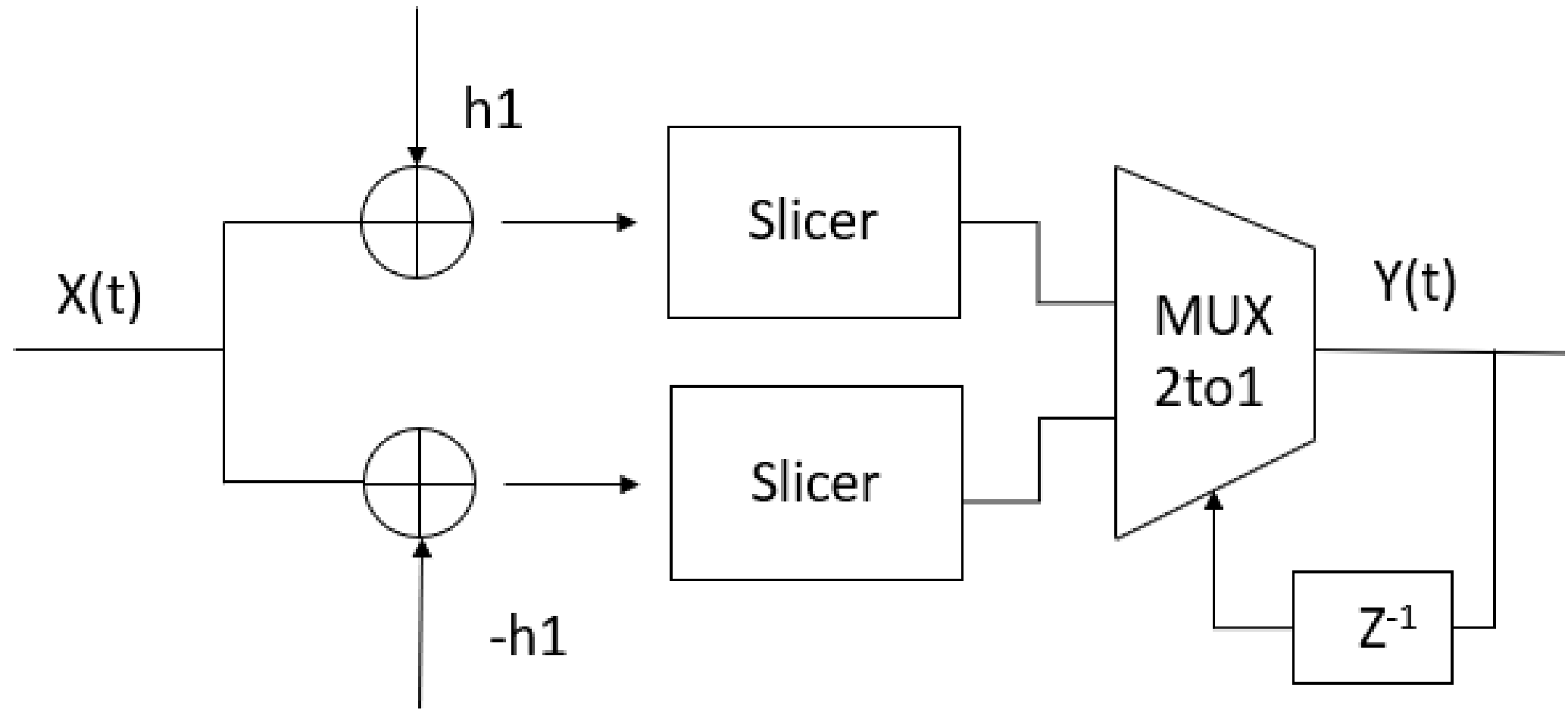


$$t_{\text{CLK-Q}} + t_{h_1} + t_{\text{SUM}} + t_{\text{setup}} < 1 \text{ UI}$$

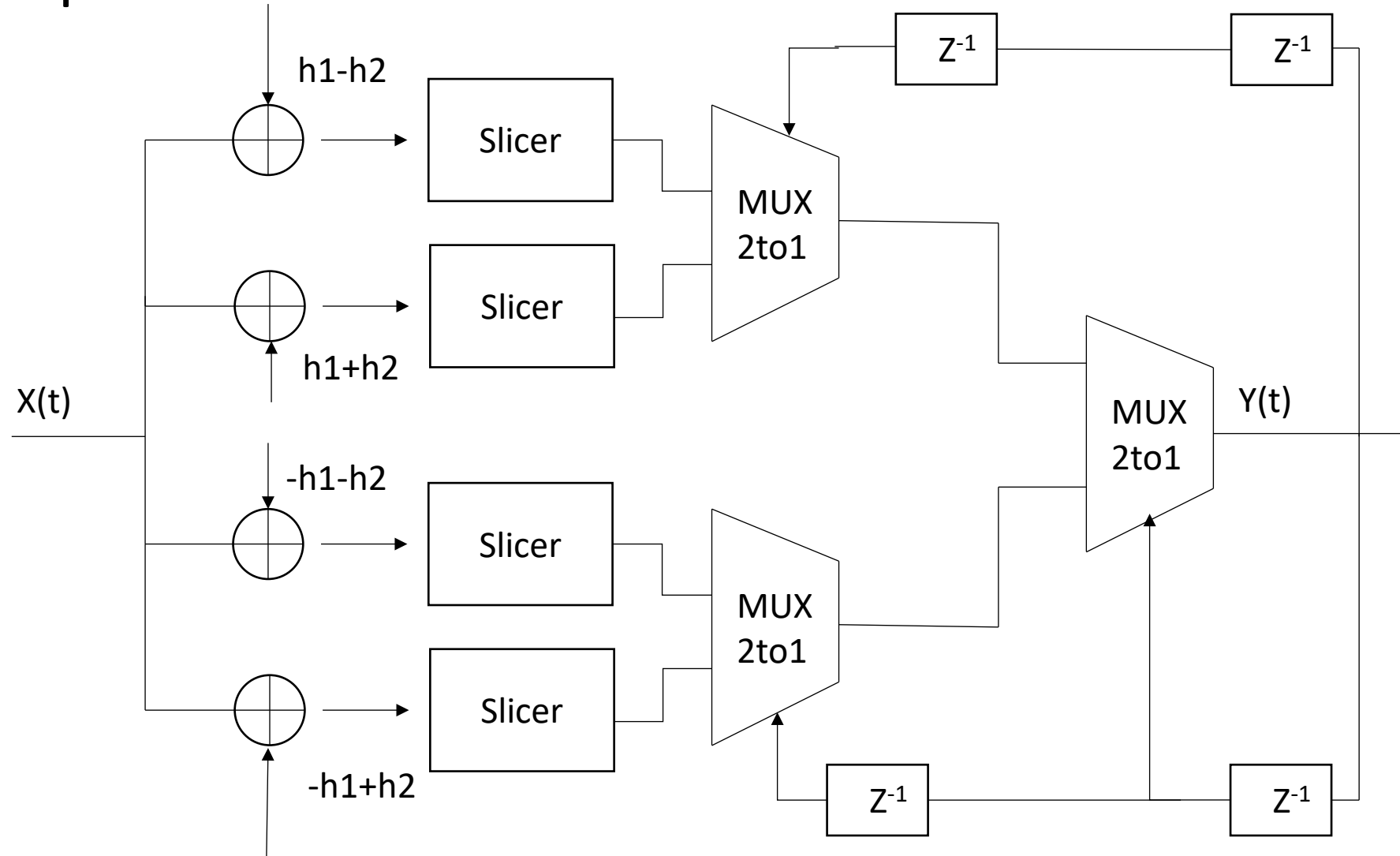
100 GBaud

1 UI = 10 ps

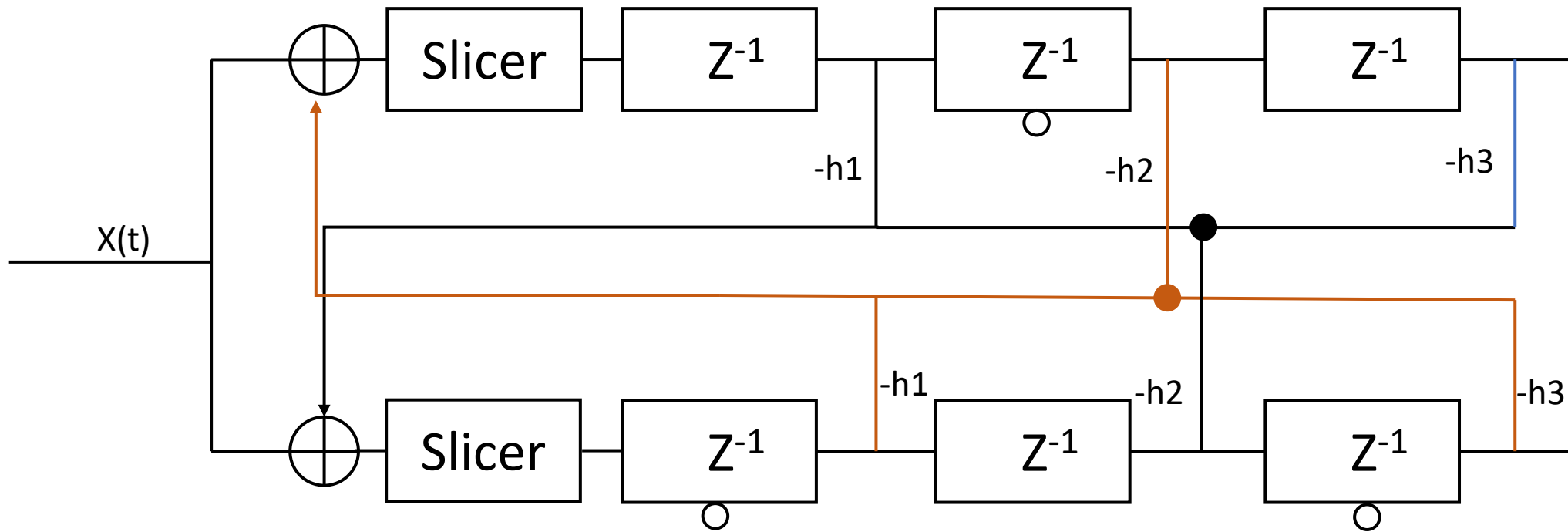
Loop-Unrolled DFE



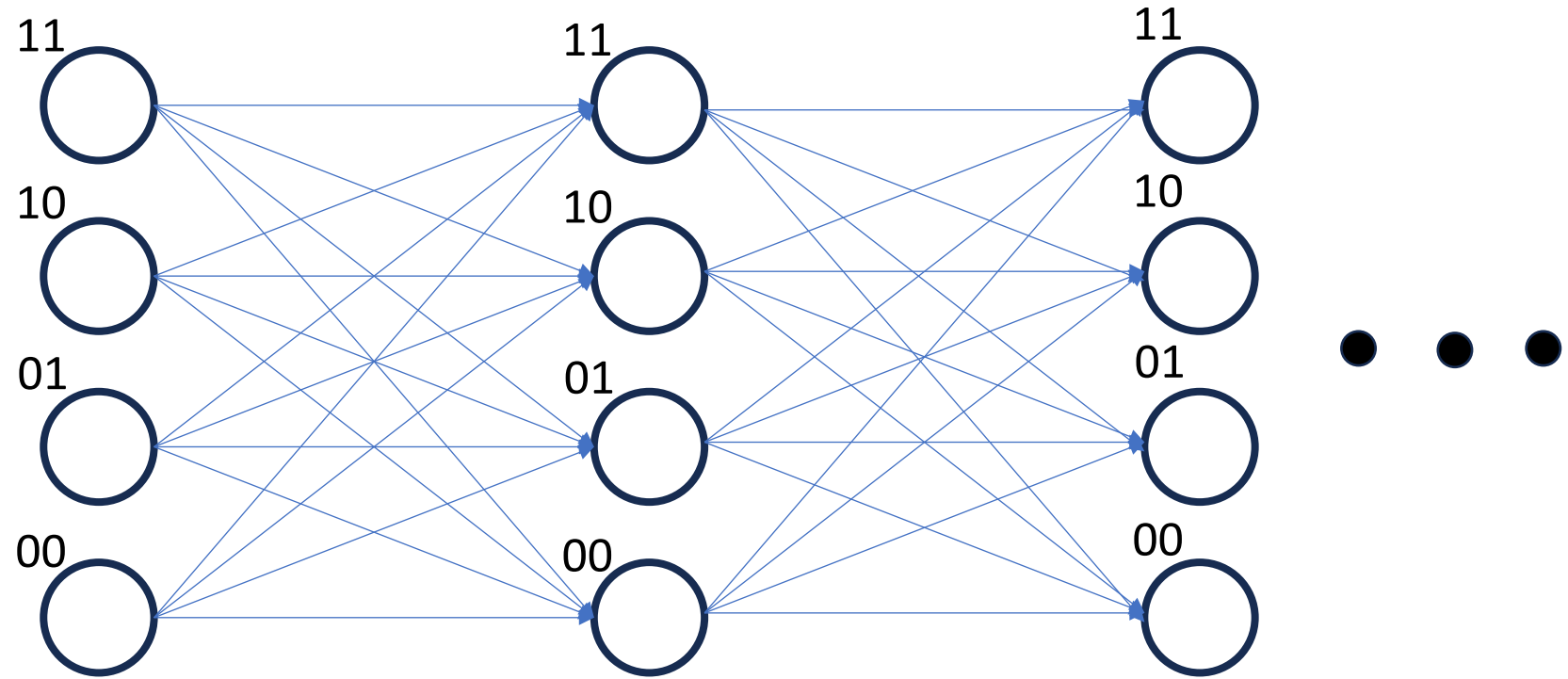
Loop-Unrolled DFE



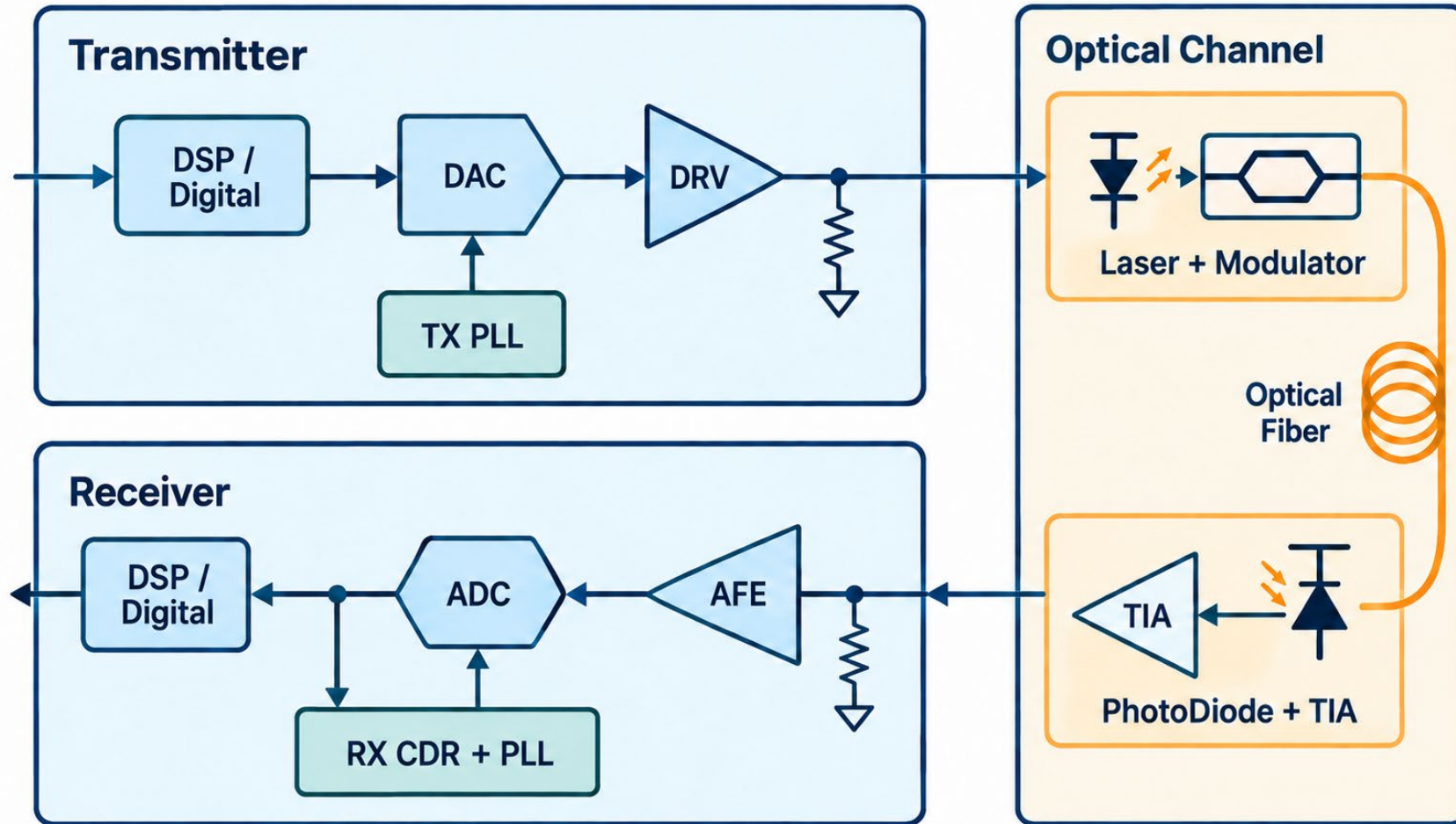
Half-rate



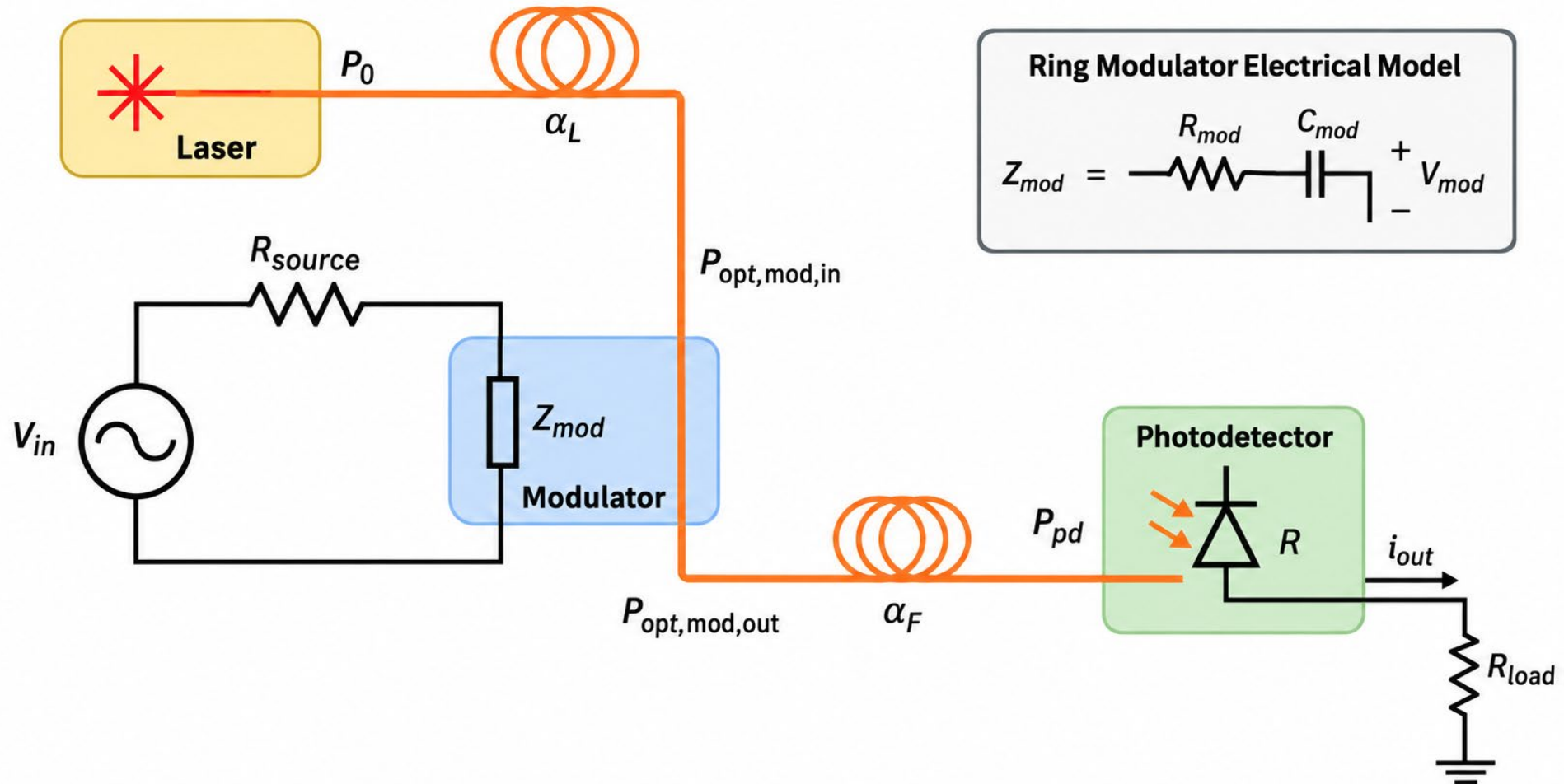
Maximum-Likelihood Sequence Detection(MLSD)



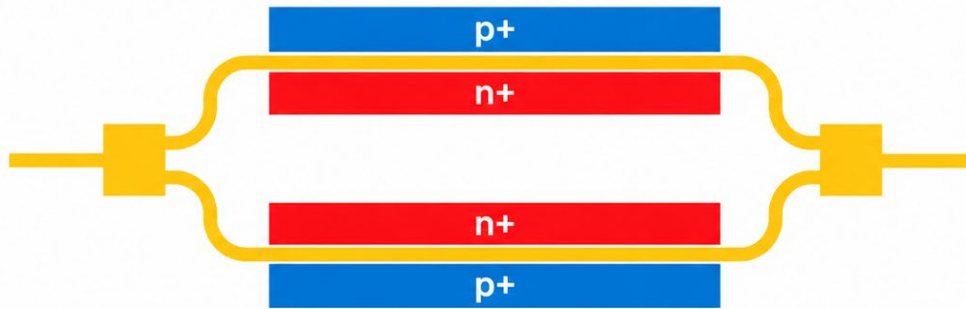
Optical Transceiver Architecture



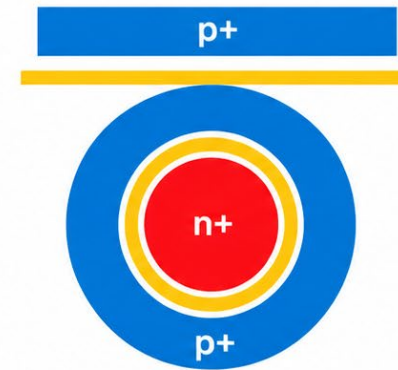
Optical Links



MZM vs MRM



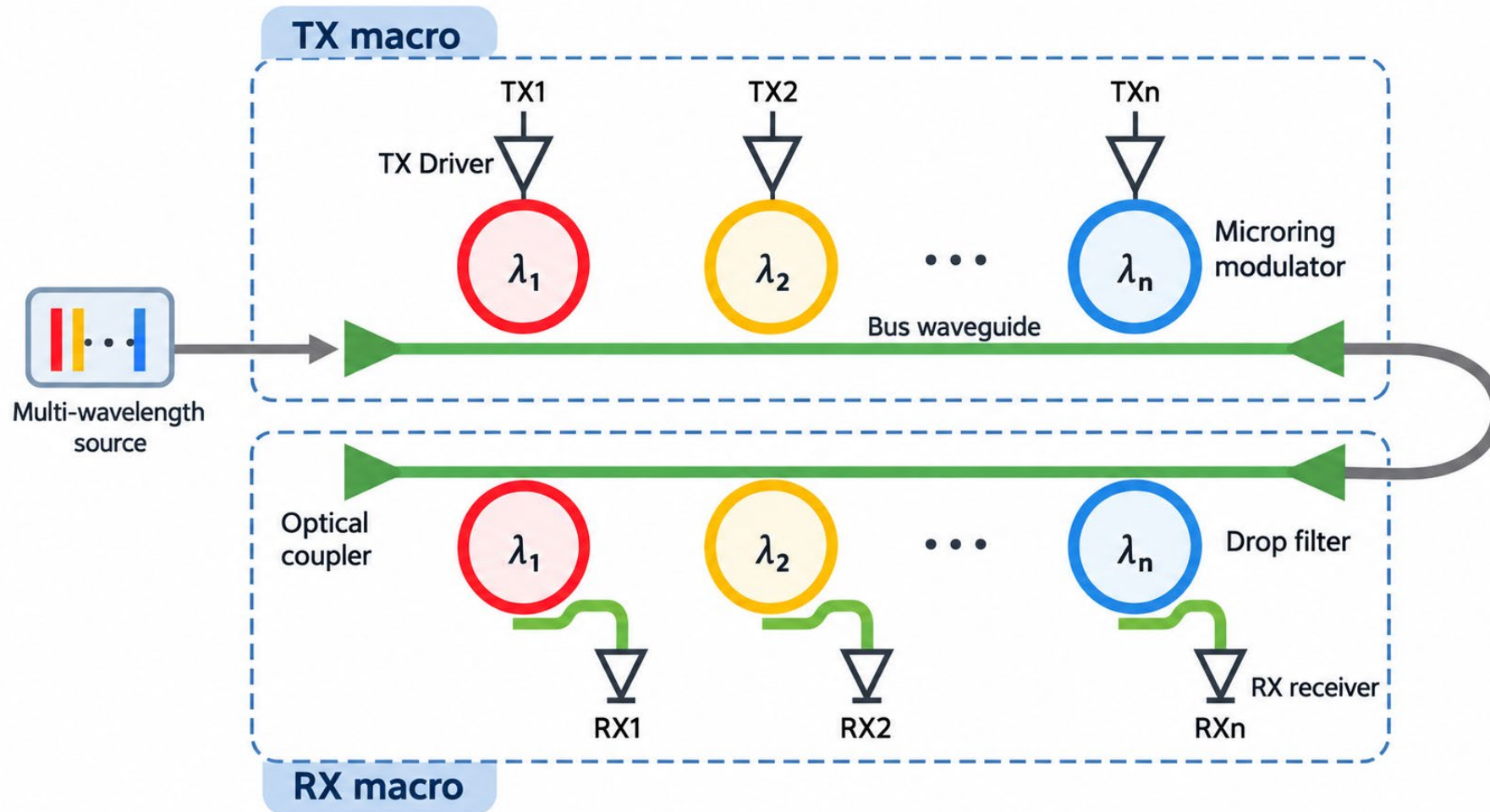
MZM



MRM

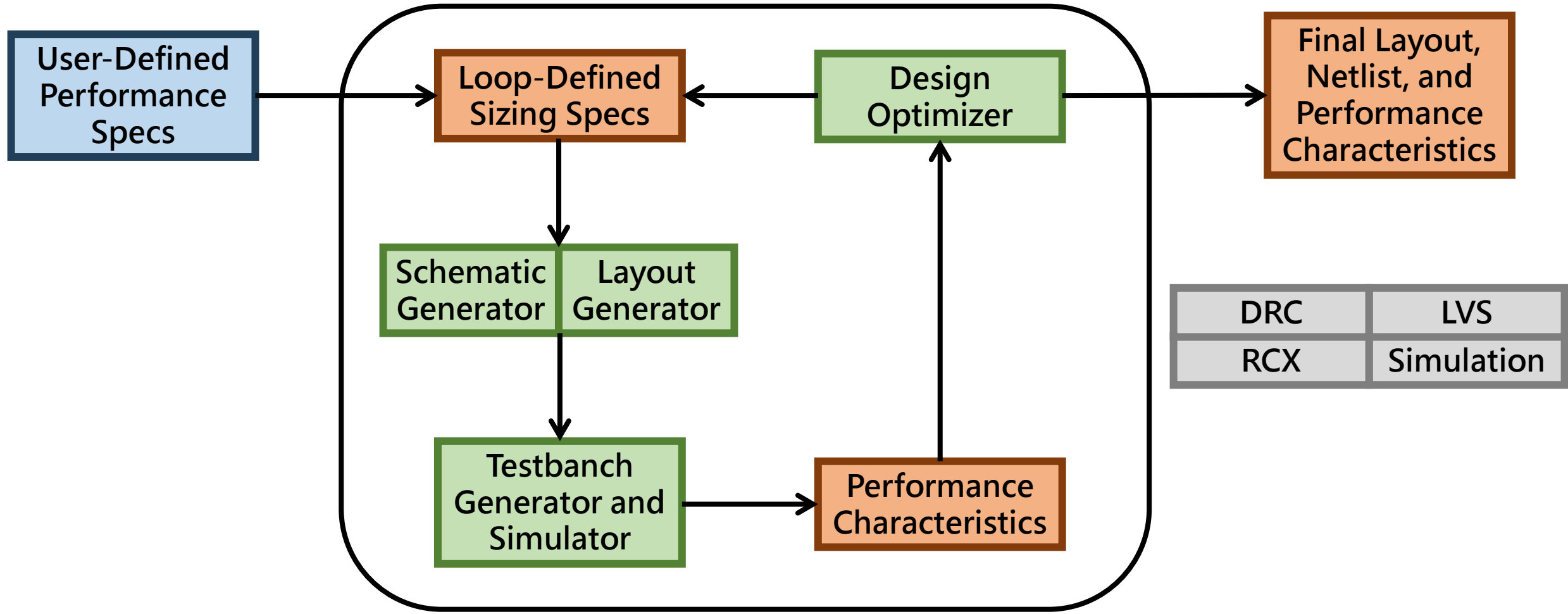
Figure of Merit	Mach Zehnder	Microring
Area	Large	Small
Extinction Ratio(ER)	Small	Large
Insertion loss	High	Low
Wavelength Sensitivity	Low	High

Wavelength Division Multiplexed Links



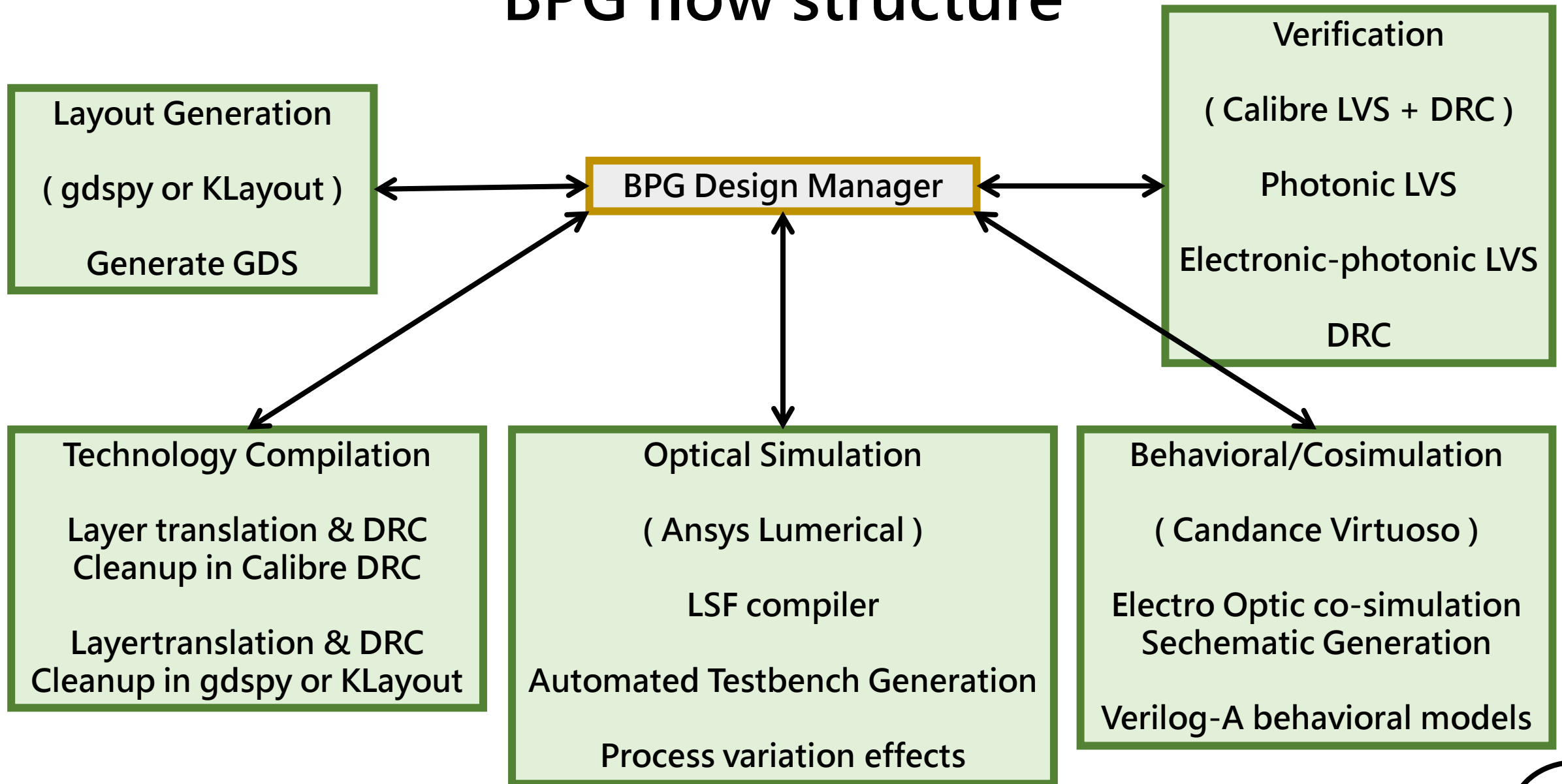
Berkeley analog generator

BAG3++ flow structure



Berkeley photonics generator

BPG flow structure



1. Why Do We Need Optical I/O?

為什麼高速運算系統不能只一直加強 electrical SerDes ?

Electrical I/O hits a bandwidth–distance wall

In-package parallel I/O : 能耗低、頻寬密度高，但 reach 只有 mm 級。

距離增加後需要高速 SerDes、equalization 與 clocking，功耗快速上升。

Pluggable optics 可以跑很遠，但傳統方案的 energy / bandwidth density 不理想。

TeraPHY 的目標：把「off-package reach」帶到接近「in-package I/O」的能耗與延遲。

Paper: ~4 orders of magnitude FOM gap between in-package and off-board solutions.

Parallel I/O

高效率 / 高頻寬密度
但 reach 很短



Electrical SerDes

距離增加 → EQ / clocking
與功耗一起上升



Pluggable Optics

長距離傳輸
但 energy / density 較差

TeraPHY TARGET

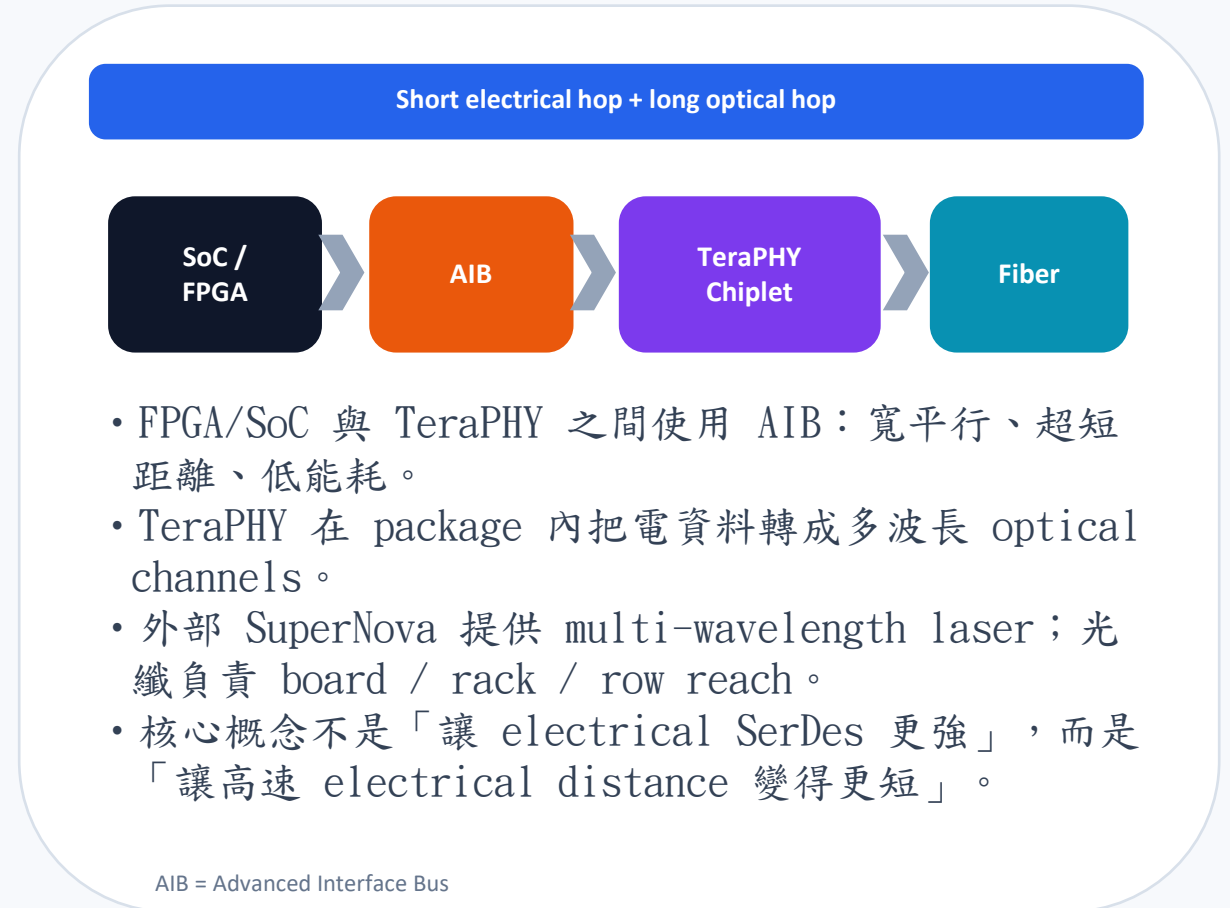
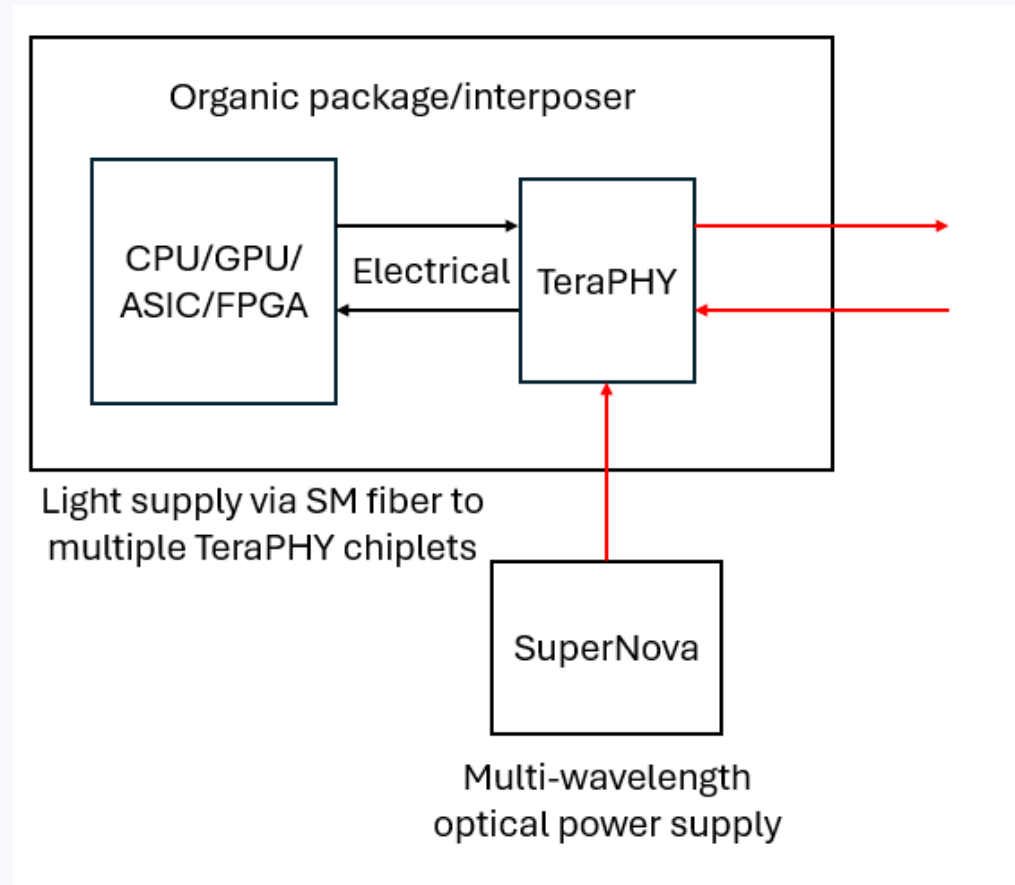
Long reach + near in-package efficiency

打破 bandwidth–distance trade-off

<https://ayarlabs.com/products/>

2. TeraPHY: Move the Optical Conversion Into the Package

TeraPHY 如何解決 bandwidth-distance trade-off



3. Two Design Pillars — BAG + BPG Co-Design

兩大設計支柱：電子電路由 BAG · 光子版圖由 BPG

① Monolithic E-P Integration

45 nm SOI CMOS



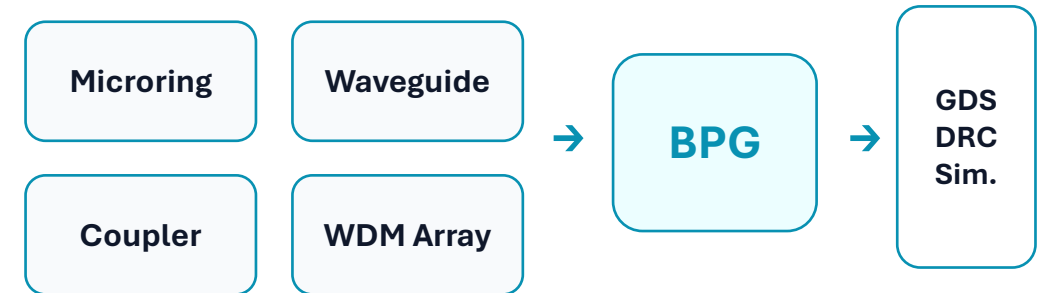
Parameterized schematic + layout

BAG connection

driver、TIA、bias / control 等電子電路的 parameterized schematic / layout generation。

② DWDM + Microrings

Many wavelengths / one waveguide



BPG connection

microrings、waveguides、couplers、WDM arrays 的 parameterized photonic layout 與驗證 flow。

Electronic-Photonic Co-Design = BAG (electronics) + BPG (photonics)

4. Key Data Breakthroughs

MEASURED TX

100 Gb/s

PAM4 / wavelength

0.7 pJ/bit

PRIOR MACRO

1.625 Tb/s

WDM Tx macro

~0.8 pJ/bit

CHIPLET I/F

960 Gb/s

AIB Tx/Rx / chiplet

24 × 40 Gb/s

SYSTEM LEVEL

<5 pJ/bit

multi-Tb/s I/O

<10 ns • up to 2 km

How to read these numbers

1 **0.7 pJ/bit @ 100 Gb/s PAM4**

optical Tx 的量測結果。

2 **960 Gb/s**

單顆 TeraPHY 的 AIB electrical interface capacity。

3 **<5 pJ/bit 、 multi-Tb/s 、 <10 ns 、 2 km**

論文結論描述的完整 optical packaging capability